

TOSHIBA THYRISTOR SILICON PLANAR TYPE

SF5GZ47, SF5JZ47

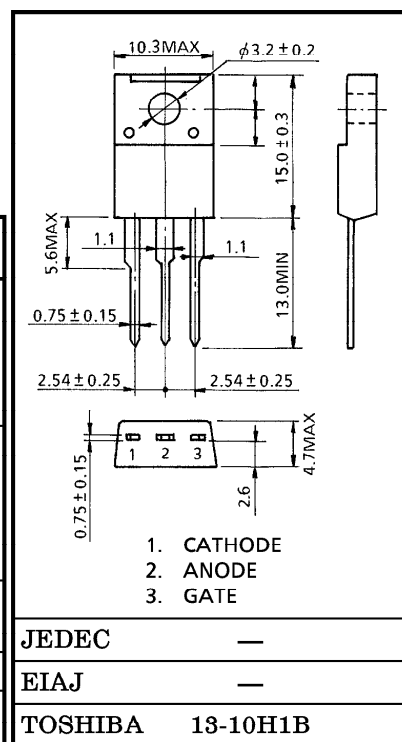
MEDIUM POWER CONTROL APPLICATIONS

Unit in mm

- Repetitive Peak off-State Voltage : V_{DRM}
- Repetitive Peak Reverse Voltage : V_{RRM}
- Average On-State Current : $I_T(AV)=5A$
- Isolation Voltage : $V_{ISOL}=1500V$ AC

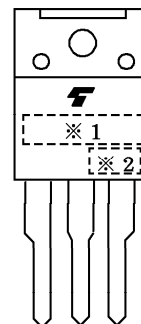
MAXIMUM RATINGS

CHARACTERISTIC		SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltage and Repetitive Peak Reverse Voltage	SF5GZ47	V_{DRM} V_{RRM}	400	V
	SF5JZ47		600	
Non-Repetitive Peak Reverse Voltage (Non-Repetitive < 5ms, $T_j = 0 \sim 125^\circ C$)	SF5GZ47	V_{RSM}	500	V
	SF5JZ47		720	
Average On-State Current (Half Sine Waveform $T_c = 85^\circ C$)		$I_T(AV)$	5	A
R. M. S. On-State Current		$I_T(RMS)$	7.8	A
Peak One Cycle Surge On-State Current (Non-Repetitive)		I_{TSM}	80 (50Hz)	A
			88 (60Hz)	
I^2t Limit Value ($t = 1 \sim 10ms$)		I^2t	32	A^2s
Critical Rate of Rise of On-State Current (Note 1)		di/dt	100	$A/\mu s$
Peak Gate Power Dissipation		P_{GM}	5	W
Average Gate Power Dissipation		$P_G(AV)$	0.5	W
Peak Forward Gate Voltage		V_{FGM}	10	V
Peak Reverse Gate Voltage		V_{RGM}	-5	V
Peak Forward Gate Current		I_{GM}	2	A
Junction Temperature		T_j	$-40 \sim 125$	$^\circ C$
Storage Temperature Range		T_{stg}	$-40 \sim 150$	$^\circ C$
Isolation Voltage (AC, $t = 1min.$)		V_{ISOL}	1500	V



Weight : 1.7g

MARK



Note1: di/dt test condition
 $V_{DRM} = 0.5 \times \text{Rated}$
 $I_{TM} \leq 15A$
 $t_{gw} \geq 10\mu s$
 $t_{gr} \leq 250ns$
 $i_{gp} = I_{GT} \times 2.0$

※1	MARK	F5GZ47	TYPE	SF5GZ47
		F5JZ47	NAME	SF5JZ47
※2	Lot Number		Example	
	□ □ Month (Starting from Alphabet A) Year (Last Number of the Christian Era)		9A : January 1989 9B : February 1989 9L : December 1989	

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ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Repetitive Peak Off-State Current and Repetitive Peak Reverse Current	I_{DRM} I_{RRM}	$V_{DRM} = V_{RRM} = \text{Rated}$	—	—	10	μA
Peak On-State Voltage	V_{TM}	$I_{TM} = 15\text{A}$	—	—	1.5	V
Gate Trigger Voltage	V_{GT}	$V_D = 6\text{V}, R_L = 10\Omega$	—	—	1.0	V
Gate Trigger Current	I_{GT}		—	—	10	mA
Gate Non-Trigger Voltage	V_{GD}	$V_D = \text{Rated} \times 2/3, T_c = 125^\circ\text{C}$	0.2	—	—	V
Critical Rate of Rise of Off-State Voltage	dv/dt	$V_{DRM} = \text{Rated}, T_c = 125^\circ\text{C}$ Exponential Rise	—	50	—	$\text{V}/\mu\text{s}$
Holding Current	I_H	$V_D = 6\text{V}, I_{TM} = 1\text{A}$	—	—	40	mA
Latching Current	I_L	$V_D = 6\text{V}, f = 50\text{Hz}, t_{gw} = 50\mu\text{s}$ $i_G = 30\text{mA}$	—	—	50	mA
Thermal Resistance	$R_{th(j-c)}$	Junction to Case	—	—	4.2	$^\circ\text{C}/\text{W}$

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